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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/785,500	02/20/2001	Kumiko Takikawa	ASA-964	6528

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EXAMINER	
YUN, EUGENE	

ART UNIT	PAPER NUMBER
2682	5

DATE MAILED: 07/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/785,500	TAKIKAWA ET AL.	
	Examiner	Art Unit	
	Eugene Yun	2682	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-21 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-21 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 20 February 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thompson et al. (US 6,510,309) in view of Tanaka (JP 57-43453).

Referring to Claim 1, Thompson teaches a wireless communications system comprising:

A filter 38 (fig. 2);

A semiconductor chip including a signal processing integrated circuit (see col. 4, lines 20-22) having an amplifier 62 (fig. 2) for receiving an output signal from said filter 42 (fig. 2);

Wherein a main surface of said semiconductor chip is provided with a plurality of electrode terminals along an edge portion thereof (see fig. 3 where it is known in the art that all semiconductor chips include a plurality of electrode terminals along an edge portion thereof); and

Wherein said amplifier has a transistor 200 (fig. 5) including a control electrode to which the output signal of said filter to be supplied, a first electrode through which a signal is outputted in accordance with the signal supplied to said control electrode, and a second electrode to which a voltage is applied (see 200 of fig. 5 noting that the electrodes simply describe the emitter, collector, and base of a transistor). Thompson does not teach the control electrode, first electrode, and second electrode of said transistor connected to said electrode terminals through wirings, respectively and wherein none of the wirings are arranged between said electrode terminals and placements of said control electrode, said first electrode and said second electrode such that wirings traverse other wirings. Tanaka teaches the control electrode, first electrode, and second electrode of said transistor connected to said electrode terminals through wirings, respectively and wherein none of the wirings are arranged between said electrode terminals and placements of said control electrode, said first electrode and said second electrode such that wirings traverse other wirings (see fig. 4 where the transistor is connected directly to the pads 2, 6, and 7 also shown along the edges in fig. 5 noted by reference numbers 2', 6' and 7'). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the teachings of Tanaka to said system of Thompson in order to reduce parasitic inductance in a wireless IC.

Referring to Claim 2, Tanaka also teaches said semiconductor chip having said edge portion and an opposite side to said edge portion, and said electrode terminals,

said transistor and a wiring through which a voltage is supplied to said transistor are in turn arranged from said edge portion towards said opposite side (see fig. 4).

Referring to Claim 3, Thompson also teaches the voltage supplied to said second electrode terminal of said transistor as a ground voltage, and the electrode terminal through which the ground voltage is supplied to said second electrode terminal of said transistor is different from the electrode terminal through which the ground voltage is supplied to electrostatic discharge protecting circuits provided for said transistor (see 200 of fig. 5 where one electrode is connected to ground).

Referring to Claim 4, Tanaka also teaches a signal transmitting circuit and the wiring through which a voltage is supplied to said signal transmitting circuit is coupled to the same electrode terminal as that of the wiring through which a voltage is supplied to a bias circuit and said electrostatic discharge protecting circuits for said amplifier (see pad 7 in fig. 4).

Referring to Claim 5, Tanaka also teaches said amplifier present on said edge portion of said semiconductor chip and arranged near the center of said edge portion (see fig. 5).

Referring to Claim 6, Tanaka also teaches said amplifier arranged at a corner part which is defined between said edge portion of said semiconductor chip and a crossing side which crosses said one edge portion (see pads 2', 6', and 7' in fig. 5).

Referring to Claim 7, Tanaka also teaches no wiring arranged between said electrode terminal and said edge portion of said semiconductor chip (see fig. 4).

Referring to Claim 8, Tanaka also teaches the wiring arranged from said electrode terminal linked with said control electrode of said transistor and one electrode of protection diodes which are provided for said transistor (see fig. 4 where it is known in the art that protection diodes are provided in most transistors today).

Referring to Claim 9, Tanaka also teaches said amplifier arranged between said edge portion of said semiconductor chip and said electrostatic discharge protecting circuit (see figs. 4 and 5).

4. Claims 10-13 and 15-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thompson and Tanaka in view of Lysejko et al. (US 6,298,246).

Referring to Claim 10, Thompson teaches a wireless communications system comprising:

A filter 38 (fig. 2);

A semiconductor chip including a signal processing integrated circuit (see col. 4, lines 20-22) having an amplifier 62 (fig. 2) for receiving an output signal from said filter 42 (fig. 2);

Wherein a main surface of said semiconductor chip is provided with a plurality of electrode terminals along an edge portion thereof (see fig. 3 where it is known in the art that all semiconductor chips include a plurality of electrode terminals along an edge portion thereof); and

Wherein said amplifier has a transistor 200 (fig. 5) including a control electrode to which the output signal of said filter to be supplied, a first electrode through which a

signal is outputted in accordance with the signal supplied to said control electrode, and a second electrode to which a voltage is applied (see 200 of fig. 5 noting that the electrodes simply describe the emitter, collector, and base of a transistor).

Thompson does not teach the control electrode, first electrode, and second electrode of said transistor connected to said electrode terminals through wirings, respectively and wherein none of the wirings are arranged between said electrode terminals and placements of said control electrode, said first electrode and said second electrode such that wirings traverse other wirings. Tanaka teaches the control electrode, first electrode, and second electrode of said transistor connected to said electrode terminals through wirings, respectively and wherein none of the wirings are arranged between said electrode terminals and placements of said control electrode, said first electrode and said second electrode such that wirings traverse other wirings (see fig. 4 where the transistor is connected directly to the pads 2, 6, and 7 also shown along the edges in fig. 5 noted by reference numbers 2', 6' and 7'). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the teachings of Tanaka to said system of Thompson in order to reduce parasitic inductance in a wireless IC.

The combination of Thompson and Tanaka does not teach the wireless communication system comprising two signal processing circuits having different wavelengths. Lysejko teaches the wireless communication system comprising two signal processing circuits having different wavelengths (see col. 5, lines 34-43). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide

the teachings of Lysejko to said system of Thompson in order to better withstand pressure to varying climatic conditions.

Referring to Claim 11, Tanaka also teaches said semiconductor chip having said edge portion and an opposite side to said edge portion, and said electrode terminals, said transistor and a wiring through which a voltage is supplied to said transistor are in turn arranged from said edge portion towards said opposite side (see fig. 4).

Referring to Claim 12, Thompson also teaches the voltage supplied to said second electrode terminal of said transistor as a ground voltage, and the electrode terminal through which the ground voltage is supplied to said second electrode terminal of said transistor is different from the electrode terminal through which the ground voltage is supplied to electrostatic discharge protecting circuits provided for said transistor (see 200 of fig. 5 where one electrode is connected to ground).

Referring to Claim 13, Thompson also teaches each amplifier of said signal processing systems and said electrostatic discharge protecting circuits connected to said amplifier are provided in one area (fig. 2);

Said one area has a contour which is surrounded with a side extending along said edge portion of said semiconductor chip, and opposite side opposite to said edge portion and sides linking said edge portion with said opposite side (fig. 3); and

Said opposite side is of a power source line and a ground line of a contour which is changed step by step (fig. 5).

Referring to Claim 15, Thompson also teaches said amplifier of each of said signal processing systems and said electrostatic discharge protecting circuits connected to said amplifier are provided in one area (fig. 2);

Said one area is provided at a predetermined interval between said edge portion of said semiconductor chip, and opposite side opposite to said edge portion (fig. 3); and

Said opposite side is of a power source line and a ground line of a contour which is changed step by step (fig. 5).

Referring to Claim 16, Tanaka also teaches a signal transmitting circuit and the wiring through which a voltage is supplied to said signal transmitting circuit is coupled to the same electrode terminal as that of the wiring through which a voltage is supplied to a bias circuit and said electrostatic discharge protecting circuits for said amplifier (see pad 7 in fig. 4).

Referring to Claim 17, Tanaka also teaches said amplifier present on said edge portion of said semiconductor chip and arranged near the center of said edge portion (see fig. 5).

Referring to Claim 18, Tanaka also teaches said amplifier arranged at a corner part which is defined between said edge portion of said semiconductor chip and a crossing side which crosses said one edge portion (see pads 2', 6', and 7' in fig. 5).

Referring to Claim 19, Tanaka also teaches no wiring arranged between said electrode terminal and said edge portion of said semiconductor chip (see fig. 4).

Referring to Claim 20, Tanaka also teaches the wiring arranged from said electrode terminal linked with said control electrode of said transistor and one electrode

of electrostatic discharge protecting which are provided for said transistor (see fig. 4 where it is known in the art that electrostatic discharge protecting are provided in most transistors today).

Referring to Claim 21, Tanaka also teaches the electrostatic discharge protecting circuit provided for said transistor connected to said first electrode and said second electrode of said transistor, respectively (see figs. 4 and 5).

5. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Thompson, Tanaka and Lysejko in view of Yamamoto et al. (US 6,308,047).

The combination of Thompson, Tanaka and Lysejko does not teach the amplifier as a low-noise amplifier. Yamamoto teaches the amplifier as a low-noise amplifier (figs. 1 and 2). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the teachings of Yamamoto to said system of Thompson in order to better reduce noise and interference.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Yun whose telephone number is (703) 305-2689. The examiner can normally be reached on 8:30am-5:30pm Alt. Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivian Chin can be reached on (703) 308-6739. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eugene Yun
Examiner
Art Unit 2682

EY

VIVIAN CHIN
SUPERVISORY PATENT EXAMINER
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6/25/04